

# **Multi-Channel Transcutaneous Cortical Stimulation System**

Contract # N01-NS-7-2365

Progress Report #13

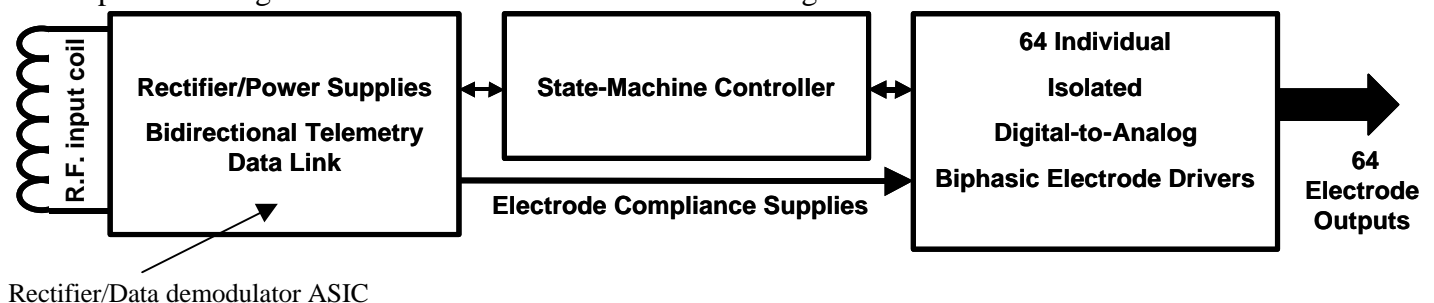
for the contract period 4/1/00 – 6/30/00

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The goal of this project is the design, fabrication, and testing of a **Multi-Channel Transcutaneous Cortical Stimulation System** to be used in a prototype artificial vision system. During the past 25 years, the development of a neuroprosthesis that could be used to restore visual sensory functions has been an important goal of the Neural Prosthesis Program (NPP) of the National Institute of Disorders and Stroke, National Institutes of Health. Demonstrations of the feasibility of a visual prosthesis have reached the stage in which the NPP is highly motivated to initiate the development of a fully implantable cortical stimulation system which could be used to provide inputs and computer control for hundreds, to over one thousand, implanted cortical electrodes. This is the thirteenth progress report for this project. In this report we describe the details and testing of the of all three ASICs used in the submodule as a combined system.

By way of review, the 64-channel submodule system architecture is shown in Figure 1, below. The Rectifier/Data demodulator ASIC's function is to rectify the stimulator's coil voltage, establish a band-gap reference and biasing for the data demodulator, clock recovery, and power supplies, recover a clock from the stimulator's coil voltage, demodulate the suspended-carrier data, provide a digital data stream and associated control signals to the State-Machine Controller. The



**Figure 11. Simplified block diagram of the 64-channel Submodule**

State-Machine Controller takes the data stream from the Rectifier/Data demodulator ASIC and decodes the mode, and address of the desired electrodes channel. The stimulus parameters for the desired channel are routed to the appropriate BLOCKCHIP. Within the BLOCKCHIP, the output of the State-Machine Controller is loaded into a serial shift register. The register is dumped into the addressed channel on the leading edge of a BLOCKCHIP latch enable. Physically, the location of the three ASICs, within the ceramic multichip module are shown in Figure 2, below.

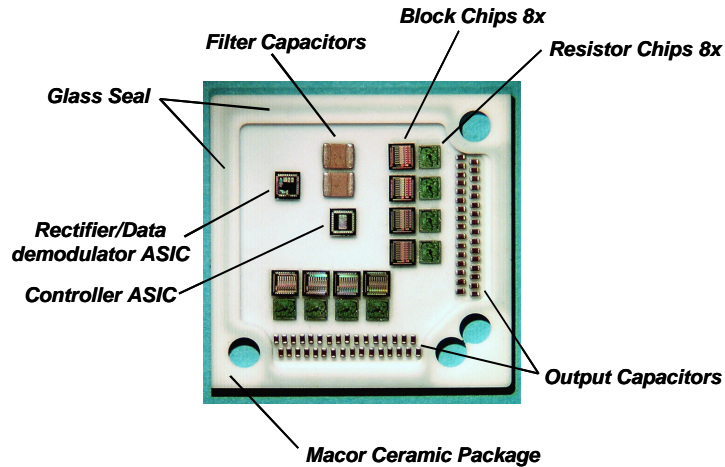


Figure 2 – Section of the 64-channel submodule showing the location of the Rectifier/Data demodulator ASIC

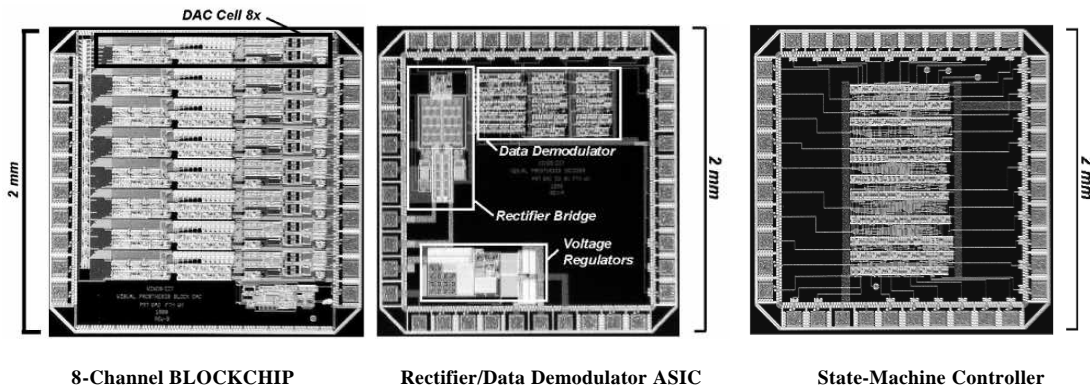


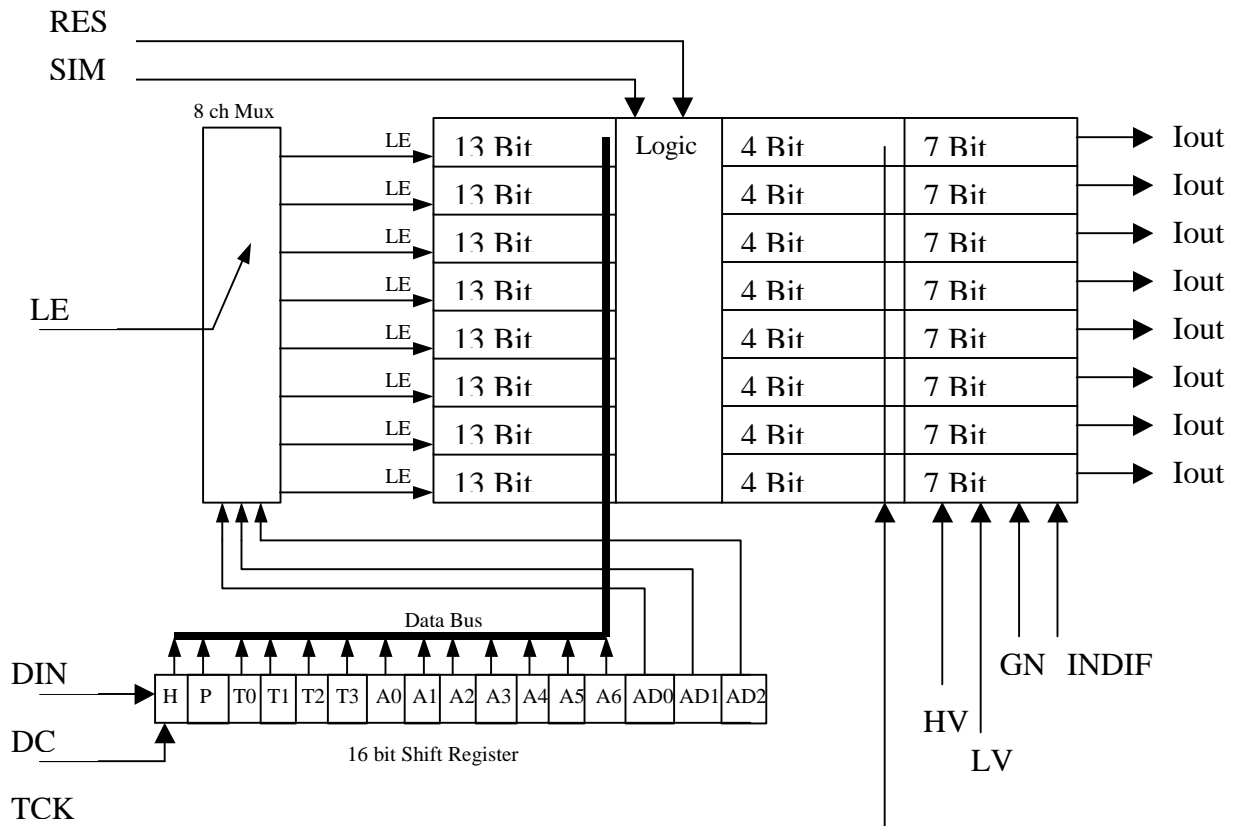
Figure 3 – Microphotographs of the ASICs used in the 64-channel Submodule

In Figure 3, above, microphotographs of each of the three ASICs, used in the 64-channel submodule are shown. These three ASICs were packaged, individually in 40-pin ceramic dip carriers. They were interconnected by means of wires on a protoboard. A prototype implant coil was connected to the Rectifier/Data Demodulator ASIC. A 5MHz suspended carrier transmitter was connected to a PC. A Labview module was written to command the transmitter in order that the appropriate data stream could be sent, over the inductive link, to the Rectifier/Data Demodulator ASIC.

The data format for the BLOCKCHIP is described below, and is included so that the nature of the data structure can be understood.

## Description of the Eight Channel Stimulator BLOCKCHIP

The BLOCKCHIP provides 8 channels of integrated biphasic stimulation capability. Each Channel consists of a 7 bit current output DAC and a 4 bit timer circuit. The DAC produces the stimulation current while the timer controls the biphasic pulse duration. In addition, a Polarity bit determines the starting polarity of the biphasic pulse, and a Holdoff bit determines whether or not stimulation will begin immediately after data is transferred to the Channel.



The chip architecture is shown in the above diagram. Incoming data is clocked into the shift register left to right. After all data bits have been clocked in, LE is asserted, and steered to the channel selected by the Mux, which causes the leftmost 13 bits of the shift register to be transferred into the 13 bit latch in the selected channel.

### Pin Description:

GND 0V reference for the logic, and power return and substrate connection for the chip.

HV 10V max. Powers the DAC circuitry and output current drivers.

LV 5V max. Powers the shift register, latches, timer and logic in the chip

**Indif** This is the reference terminal for the Iout current outputs. This would typically be held midway between HV and GND by an external voltage. It could be connected to LV as well.

**Iout** These are the stimulation current outputs. The current may be set from 0.5uA to 64uA in 0.5uA increments. The device will always produce symmetric biphasic pulses, i.e. a pulse of 30uA source current will be followed immediately and automatically by a pulse of 30uA sink current of identical duration. After both halves of the biphasic pulse have been completed, Iout will either source or sink a maximum of 0.5uA as required to reduce the voltage between the Iout terminal and the INDIF terminal to 0V. As Iout approaches INDIF, this “balancing” current is proportionally reduced to zero. This “balancing current” is intended to remove any residual voltage on the Iout terminal caused by any imbalance in the source and sink phases of the biphasic pulse.

**RESB** A low logic level on RESB will reset the timer and state machine logic of all the channels, thereby immediately terminating any stimulation pulses currently in process. RESB does not affect the contents of the latches or shift register. This line is intended to be held low during system power up to prevent spurious stimulation.

**TCLK** This is the timebase for the timers in the channels. It may be asynchronous with DCK. Simulation shows the maximum TCK rate to be around 4MHz. The timers may be programmed from 0001binary to 0000binary, thereby giving pulses with widths from 1 to 16 units of time. This is the width of one half of the biphasic pulse. TCK is divided by 16 to produce the width step size, e.g if TCK=1MHz, a timer setting of 0001binary will produce a positive current pulse 16uS long immediately followed by a negative current pulse 16uS long.

**DIN** This is the Data input to the shift register.

**DCK** This is the clock input to the shift register. According to simulation, DCK can run to about 4MHz. The logic level on DIN is clocked into the shift register on the rising edge of DCK.

**LE** The rising edge of LE sets a flip-flop. On the next rising edge of TCK, the 13 bit data latch of the selected channel loads the data from the shift register. The channel is selected by the Muc, which takes as the channel address the rightmost three bits contained within the shift register. To insure a proper data load into the proper channel, the shift register contents must be stable until after the first rising edge of TCK after the rising edge of LE.

**SIM** The rising edge of SIM sets a flip-flop. On the next rising edge of TCK, any channel in the block chip which has in its 13 bit register its Holdoff bit (H) set will emit a stimulation pulse according to the parameters stored in its 13 bit latch. This way, any number of channels in the block chip may be made to stimulate simultaneously.

## Data Description

### AD2, AD1, AD0

The channel address, 0 to 7 (000b to 111b) determines in which channel the pulse parameters will be stored after the next LE pulse.

### A6 through A0

Stimulation amplitude, 128 steps in 0.5uA increments (0uA to 63.5uA). A value of 0000000b results in no stimulation pulse. Also, with a programmed amplitude value of 0, the timer is never started, so that channel may be immediately reprogrammed and stimulated without having to wait for the channel timer to complete its cycle.

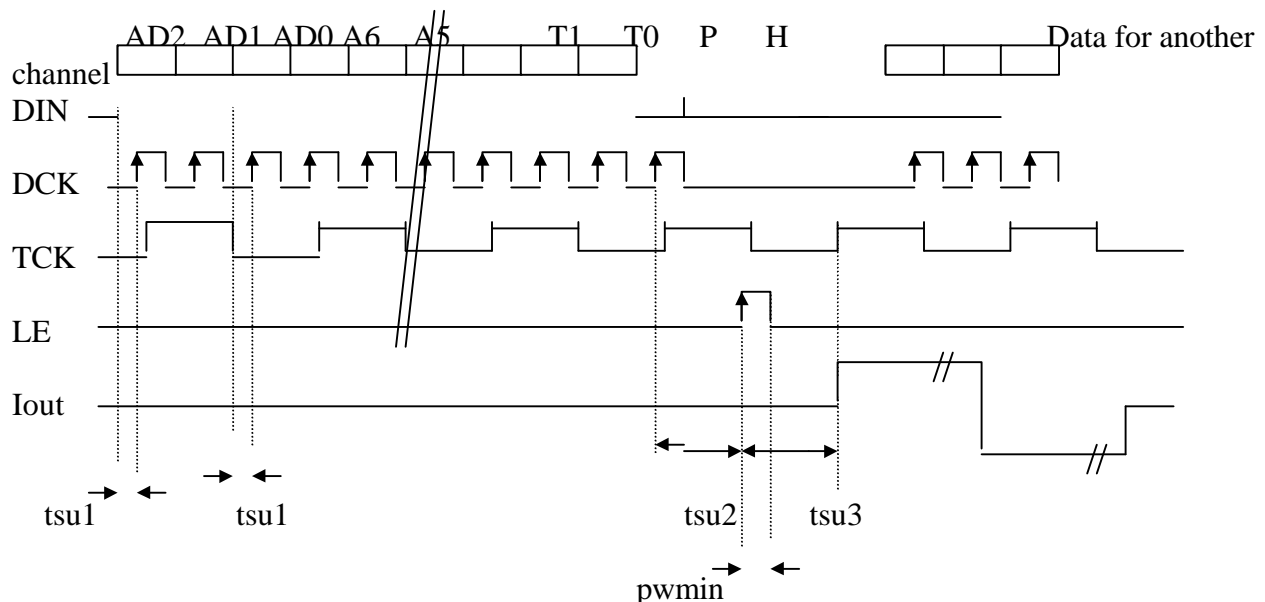
### T3 through T0

Pulse width. This is the width of one half the biphasic pulse. The time increment is 16 times the period of TCK. The shortest time is when T3,T2,T1,T0 = 0001b, the next shortest is 0010b, all the way up to 0000b, which produces a pulse of 16 times the shortest pulse. Once the timer starts counting and the channel is producing the specified pulse, further attempts to load data to the 13 bit latch within that channel are inhibited until the timer completes its entire cycle, or the RESB line is brought low to reset the timers and logic in all channels on the chip.

**P** The Polarity bit. If set to one, the biphasic pulse will start with Iout sourcing current. If 0, the pulse will start with Iout sinking current.

**H** The Holdoff bit. If set to 0, stimulation will begin on the next rising edge of TCK after the rising edge of LE. If set to 1, stimulation will not begin until the next rising edge of TCK after SIM is asserted. In other words, a channel will stimulate as soon as the data is loaded into the channel unless the Holdoff bit is set.

### Typical Timing, Holdoff bit not set



tsu1= The minimum time data must be present on DIN before the occurrence of the rising edge of DCK. This time will be approximately 200nS.

tsu2= The minimum time between the clocking in of the last data bit and the rising edge of LE. This time will also be approximately 200nS.

tsu3= The minimum time between the rising edge of LE and the rising edge of TCK. This time will also be approximately 200nS, however since TCK may be asynchronous with LE, if tsu3 is not met, stimulation will begin normally on the next rising edge of TCK.

pwmin= The minimum LE pulse width is approximately 100nS.

### **Specific Timing**

In the implant, all internal clock frequencies will be derived from the excitation carrier frequency. The internal dividers in the implant and the exact carrier frequency will be chosen to insure the timing requirement of 50uS pulse time increments will be met, and the data transfer rate is sufficiently high to support the required update rates. Although the block chip places no restrictions on any synchronization between DCK and TCK, these rates will ultimately be derived from the carrier frequency. In the implant, the timing will be as follows:

TCK must be 320,000.00Hz to produce pulse width time increments of 50uS.

The carrier frequency will be  $14 * TCK = 4.480\text{MHz}$

Using 4 carrier cycles/Bit for the data modulation, the DIN data stream will come in at 1.120MBPS, DCK will therefore be 1.120 MHz

Depending upon the dynamics of our magnetic link, it may be possible to double the data transfer rate by using only 2 carrier cycles/bit for our data modulation. In this case, DIN and DCK will double to 2.240MHz.

### **Testing of the Combined System.**

Commands were issued, via the PC, to the transmitter. The output of the BLOCKCHIP was observed on a multichannel oscilloscope as the stimulus parameters were adjusted. All channels appropriately responded to the computer commands. Two versions of the State-Machine Controller were tested: one that used parity checking, and one that did not. It was interesting to see that there were no observed errors in the stimulus outputs when using the non-parity checking ASIC. It is likely that there may have been intermittent cycles of error, that did not show up on the repetitive oscilloscope waveforms. The initial prototype of the parity-checking version of the State-Machine Controller had a design flaw. This was corrected in a subsequent fabrication run, and the latest version of this ASIC functions as expected.

In summary, we have several second-order effects, within the BLOCKCHIP that we intend to correct on future wafer fabrication runs. However, all of the electronic chips are functional and provide the basis for a complete 256-channel stimulation module.

